WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a plurality of memory cells arranged in a matrix of rows and columns;

a plurality of word lines arranged corresponding to a plurality of rows in said plurality of memory cells;

a plurality of bit line pairs arranged corresponding to a plurality of columns in said plurality of memory cells;

a plurality of sense amplifier zones detecting and amplifying data read from said plurality of memory cells; and

a plurality of sub-word line driver zones intersecting each of said plurality of sense amplifier zones; wherein

each of said plurality of sense amplifier zones includes

a plurality of sense amplifiers provided corresponding to said plurality of bit line pairs and detecting and amplifying a potential difference between the corresponding bit line pair,

a sense amplifier driving line provided in common to said plurality of sense amplifiers, and

a plurality of first data line pairs provided corresponding to said plurality of bit line pairs and each selectively connected to a corresponding bit line;

the semiconductor memory device further comprises a plurality of sub-amplifiers provided corresponding to each of said plurality of first data line pairs;

each of said plurality of sub-amplifiers includes first, second, and third transistors;

said first transistor has a control terminal connected to one line of said first data line pair, a first conductive terminal connected to another line of said first data line pair, and a second conductive terminal connected to a first conductive terminal of said third transistor;

said second transistor has a control terminal connected to another line of said first data line pair, a first conductive terminal connected to one

line of said first data line pair, and a second conductive terminal connected to the first conductive terminal of said third transistor; and

said third transistor has a control terminal receiving an activation timing control signal for said sub-amplifier, and a second conductive terminal connected to said sense amplifier driving line.

2. A semiconductor memory device, comprising:

a plurality of memory cells arranged in a matrix of rows and columns;

a plurality of word lines arranged corresponding to a plurality of rows in said plurality of memory cells;

a plurality of bit line pairs arranged corresponding to a plurality of columns in said plurality of memory cells;

a plurality of sense amplifier zones detecting and amplifying data read from said plurality of memory cells; and

a plurality of sub-word line driver zones intersecting each of said plurality of sense amplifier zones; wherein

each of said plurality of sense amplifier zones includes

a plurality of sense amplifiers provided corresponding to said plurality of bit line pairs and detecting and amplifying a potential difference between the corresponding bit line pair,

a sense amplifier driving line provided in common to said plurality of sense amplifiers, and

a plurality of first data line pairs provided corresponding to said plurality of bit line pairs and each selectively connected to a corresponding bit line;

each of said plurality of sub-word line driver zones includes a plurality of second data line pairs provided corresponding to said plurality of first data line pairs and receiving data amplified via said sub-amplifier of corresponding said first data line pair in reading;

the semiconductor memory device further comprises a plurality of sub-amplifiers provided corresponding to each of said plurality of first data line pairs;

each of said plurality of sub-amplifiers includes first, second, and third transistors;

said first transistor has a control terminal connected to one line of said first data line pair, a first conductive terminal connected to one line of said second data line pair, and a second conductive terminal connected to a first conductive terminal of said third transistor;

said second transistor has a control terminal connected to another line of said first data line pair, a first conductive terminal connected to another line of said second data line pair, and a second conductive terminal connected to the first conductive terminal of said third transistor; and

said third transistor has a control terminal receiving an activation timing control signal for said sub-amplifier, and a second conductive terminal connected to said sense amplifier driving line.

3. The semiconductor memory device according to claim 1, further comprising

a column decoder generating a column selection signal selecting said bit line pair connected to each of said plurality of first data line pairs in response to an address signal, and

a control signal generating circuit outputting an activation timing control signal for said sub-amplifier, upon receiving a column selection enable signal activating said column decoder, wherein

said control signal generating circuit includes a delay circuit delaying activation of said activation timing control signal for said sub-amplifier until a time point after said column selection signal is activated.

4. The semiconductor memory device according to claim 2, wherein

a column decoder generating a column selection signal selecting said bit line pair connected to each of said plurality of first data line pairs in response to an address signal, and

a control signal generating circuit outputting an activation timing control signal for said sub-amplifier, upon receiving a column selection enable signal activating said column decoder, wherein

said control signal generating circuit includes a delay circuit delaying activation of said activation timing control signal for said sub-amplifier until a time point after said column selection signal is activated.

5. The semiconductor memory device according to claim 2, wherein

said sub-amplifier further includes an input/output switching circuit controlling connection/isolation between said first data line pair and said second data line pair, and

said input/output switching circuit includes

an NAND circuit having an inverted signal of said activation timing control signal for said sub-amplifier and an input/output switching signal input,

an inverter inverting an output from said NAND circuit, and

first and second transfer gate circuits connecting/isolating said first data line pair to/from said second data line pair, in response to an input/output of said inverter.

6. The semiconductor memory device according to claim 1, wherein

each of said plurality of sub-amplifiers is provided in a region where said plurality of sense amplifier zones cross said plurality of sub-word line driver zones.

7. The semiconductor memory device according to claim 2, wherein

each of said plurality of sub-amplifiers is provided in a region where said plurality of sense amplifier zones cross said plurality of sub-word line driver zones.